REMARKS

Claims 1, 3-5 and 7-8 are currently pending in the present application.

Rejection under 35 U.S.C. § 103

Claims 1, 4-5 and 8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Devlin et al.* (US 6,710,621) in view of *Gheewala* (US 6,091,090). Applicant respectfully traverses such rejection.

Under MPEP § 706.02(j), in order to establish a *prima facie* case of obviousness, three criteria must be met. First, there must be some suggestion or motivation to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art references must teach or suggest all the claimed limitations.

Claim 1 recites "reserving metal layer M1 for power supply bus when developing a bus structure of an ASIC device image" and "adding power supply bus for said power supply voltages to metal layer M1 in said logic blocks." It is clear that the claimed adding step is closely related to the claimed reserving step because without the claimed reserving step, the claimed adding step would not have the same result for the power supply bus. On page 3 of the Final Office Action, the Examiner states that the claimed reserving step is not taught or suggested by *Devlin*; however, the Examiner asserts that the claimed reserving step is disclosed by *Gheewala* in col. 1, line 65 - col. 2, line 3.

Assuming *arguendo* that *Gheewala* does disclose the claimed reserving step, but the Examiner has not provided any suggestion or motivation to combine the teachings of *Gheewala* and *Devlin*. For example, on page 4 of the Final Office Action, the Examiner states that "*Gheewala* discloses that an advantage of reserving the M1 metal layer for power supply trace is that a direct connection can be made between power supply trace and diffusion regions without additional metal routing-[col.2, line[sic] 8 - 13]." In col. 2, lines 8 - 13, *Gheewala* simply states that

> Most commonly, power supply traces **130** and **132** are connected to diffusion region **105** and **107** at a common node between the two transistors by contacts **140** and **142**. An advantage of this layout is that a direct connection can be made between power supply trances **130** and **132** and diffusion regions **105** and **107**, without additional metal routing.

The advantage *Gheewala* is referring to is that "power supply traces **130** and **132** are connected to diffusion region **105** and **107** at a common node between the two transistors by contacts **140** and **142**" and not "reserving the M1 metal layer," as suggested by the Examiner.

In fact, *Gheewala* actually teaches away from using M1 metal layer as power supply bus. *Gheewala* describes the traditional method of routing power supply traces in col. 2, lines 14-21, and then explains the disadvantage of the traditional method of routing power supply traces in col. 2, lines 22-31. *Gheewala*'s improved method of routing power supply traces is succinctly described in the ABSTRACT section as follows:

> Local interconnection and global interconnections are routed on the first metal layer in a direction parallel to the rows (horizontal). Power supply signals and global interconnection are routed in the second metal layer in a direction parallel to the rows (horizontal). Global interconnections are routed on the third metal layer in a direction parallel to the columns (vertical).

Since *Gheewala* teaches that power supply signals should not be routed in the M1 metal layer, and that power supply signals should be routed in the M2 metal layer; thus, *Gheewala* clears teaches away from the claimed steps of reserving and adding power supply bus to metal layer M1.

As such, there would not be any expectation of success by combining teachings of *Gheewala* and *Devlin* to render the claimed invention obvious for the purpose of the § 103 rejection. Because the cited references, whether considered separately or in combination, do not teach or suggest all the features of the claimed invention, the § 103 rejection is believed to be overcome.

CONCLUSION

Claims 1, 3-5 and 7-8 are currently pending in the present application. For the reasons stated above, Applicant believes independent Claims 1 and 5, and all their respective dependent claims are distinguished over the cited references under § 103, and should be in condition for allowance. The remaining prior art cited by the Examiner, but not relied upon, has been reviewed and is not believed to show or suggest the claimed invention.

No fee or extension of time is believed to be necessary; however, in the event that any fee or extension of time is required for the prosecution of the present application, please charge it against BAE Systems Deposit Account No. **19-0130**.

Respectfully submitted,

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